



AXP805 Datasheet

PMIC for Multi-Core High-Performance System

Version 1.0

Nov.14, 2017

Declaration

THIS DOCUMENTATION IS THE ORIGINAL WORK AND COPYRIGHTED PROPERTY OF X-POWERS. REPRODUCTION IN WHOLE OR IN PART MUST OBTAIN THE WRITTEN APPROVAL OF X-POWERS AND GIVE CLEAR ACKNOWLEDGEMENT TO THE COPYRIGHT OWNER.

THE PURCHASED PRODUCTS, SERVICES AND FEATURES ARE STIPULATED BY THE CONTRACT MADE BETWEEN X-POWERS AND THE CUSTOMER. PLEASE READ THE TERMS AND CONDITIONS OF THE CONTRACT AND RELEVANT INSTRUCTIONS CAREFULLY BEFORE USING, AND FOLLOW THE INSTRUCTIONS IN THIS DOCUMENTATION STRICTLY. X-POWERS ASSUMES NO RESPONSIBILITY FOR THE CONSEQUENCES OF IMPROPER USE(INCLUDING BUT NOT LIMITED TO OVERVOLTAGE, OVERCLOCK, OR EXCESSIVE TEMPERATURE).

THE INFORMATION FURNISHED BY X-POWERS IS PROVIDED JUST AS A REFERENCE OR TYPICAL APPLICATIONS. ALL STATEMENTS, INFORMATION, AND RECOMMENDATIONS IN THIS DOCUMENT DO NOT CONSTITUTE A WARRANTY OF ANY KIND, EXPRESS OR IMPLIED. X-POWERS RESERVES THE RIGHT TO MAKE CHANGES IN CIRCUIT DESIGN AND/OR SPECIFICATIONS AT ANY TIME WITHOUT NOTICE.

NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THE THIRD PARTIES WHICH MAY RESULT FROM ITS USE. NO LICENSE IS GRANTED BY IMPLICATION OR OTHERWISE UNDER ANY PATENT OR PATENT RIGHTS OF X-POWERS. THIRD PARTY LICENCES MAY BE REQUIRED TO IMPLEMENT THE SOLUTION/PRODUCT. CUSTOMERS SHALL BE SOLELY RESPONSIBLE TO OBTAIN ALL APPROPRIATELY REQUIRED THIRD PARTY LICENCES. X-POWERS SHALL NOT BE LIABLE FOR ANY LICENCE FEE OR ROYALTY DUE IN RESPECT OF ANY REQUIRED THIRD PARTY LICENCE. X-POWERS SHALL HAVE NO WARRANTY, INDEMNITY OR OTHER OBLIGATIONS WITH RESPECT TO MATTERS COVERED UNDER ANY REQUIRED THIRD PARTY LICENCE.

Revision History

Revision	Date	Description
1.0	Nov.14, 2017	Initial release Version

Contents

1. Overview	6
2. Feature	7
3. Typical Application	8
4. Block Diagram	9
5. Pin Description	10
6. Absolute Maximum Ratings	13
7. Electrical Characteristics	14
8. Control and Operation	19
8.1. Master mode	20
8.2. Slave mode.....	20
8.3. Self-work mode.....	21
8.4. Sleep and Wakeup	22
8.5. Reference、Internal Power and Interrupt.....	23
8.6. Multi-Power Outputs	24
8.7. Serial Interface	25
9. Register	26
9.1. Register List	26
9.2. Register Description.....	27
9.2.1. REG 00: Startup Source	27
9.2.2. REG 03: IC Type NO.	27
9.2.3. REG 04-07: 4 Data Buffers.....	27
9.2.4. REG 10: Output Power on-off Control 1.....	27
9.2.5. REG 11: Output Power on-off Control 2.....	28
9.2.6. REG 12: DCDC-A Voltage Control	28
9.2.7. REG 13: DCDC-B Voltage Control	28
9.2.8. REG 14: DCDC-C Voltage Control	29
9.2.9. REG 15: DCDC-D Voltage Control	29
9.2.10. REG 16: DCDC-E Voltage Control.....	29
9.2.11. REG 17: ALDO1 Voltage Control.....	29
9.2.12. REG 18: ALDO2 Voltage Control.....	29
9.2.13. REG 19: ALDO3 Voltage Control.....	30
9.2.14. REG 1A: DCDC Mode Control 1	30
9.2.15. REG 1B: DCDC Mode Control 2	30
9.2.16. REG 1C: DCDC Frequency Setting.....	30
9.2.17. REG 1D: Output Monitor Control.....	31
9.2.18. REG 1F: IRQ & PWROK& Off Discharge Setting.....	31
9.2.19. REG 20: BLDO1 Voltage Control	32
9.2.20. REG 21: BLDO2 Voltage Control	32
9.2.21. REG 22: BLDO3 Voltage Control	32
9.2.22. REG 23: BLDO4 Voltage Control	33
9.2.23. REG 24: CLDO1 Voltage Control	33
9.2.24. REG 25: CLDO2 Voltage Control	33
9.2.25. REG 26: CLDO3 Voltage Control	33
9.2.26. REG 31: Power Wakeup Ctrl & VOFF Setting.....	33

9.2.27. REG 32: Power Disable & Power Down Sequence	34
9.2.28. REG 35: Wakeup Pin Function Setting	35
9.2.29. REG 36: POK Setting.....	35
9.2.30. REG 3E: Interface Mode Select	35
9.2.31. REG 3F: Special Control Register.....	36
9.2.32. REG 40: IRQ Enable1	36
9.2.33. REG 41: IRQ Enable2	36
9.2.34. REG 48: IRQ Status1	37
9.2.35. REG 49: IRQ Status2	37
9.2.36. REG F3: VREF & Temperature Warning Level Setting.....	37
9.2.37. REG FE: Serial Interface Address Extension.....	38
9.2.38. REG FF: Register Address Extension	38
10. Package	39

1. Overview

AXP805 is a highly integrated power management IC(PMIC) for 5V inputs and it provides multiple high current power supply. For high-performance multi-core system, AXP805 comes with multi-phase power supply that supports up to 7.5A of current output. It also works with power management chips with battery management capabilities to provide a complete power management solution for power supply system.

AXP805 supports 15 channels power outputs, which includes 5 channels adjustable output buck DC-DC, 10 channels adjustable output LDO. To ensure the security and stability of the power system, AXP805 provides protection circuits such as over-voltage protection(OVP), under-voltage protection(UVP), over-current protection(OCP) and over-temperature protection(OTP), and it provides a high-speed serial interface at the same time, so that the application processor can easily adjust the output voltage of each channel.

AXP805 is available in 7mm x 7mm 56-pin QFN package.

2. Feature

- **5-CH DCDC**
 - DCDC-A: PFM/PWM
0.6V~1.1V, 10mV/step, 51steps;
1.12V~1.52V, 20mV/step, 21steps;
IMAX = 2.5A
 - DCDC-B: PFM/PWM
1.0V~2.55V, 50mV/step, 32steps;
IMAX = 2.5A
 - DCDC-C: PFM/PWM
0.6V~1.1V, 10mV/step, 51steps;
1.12V~1.52V, 20mV/step, 21steps;
IMAX = 2.5A
 - DCDC-D: PFM/PWM
0.6V~1.5V, 20mV/step, 46steps;
1.6V~3.3V, 100mV/step, 18steps;
IMAX = 1.5A
 - DCDC-E: PFM/PWM
1.1V~3.4V, 100mV/step, 24steps;
IMAX = 1.5A
 - ALDO3: 0.7V~3.3V, 100mV/step, 27steps,
IMAX = 300mA, Input Power is ALDOIN
 - BLDO1: 0.7V~1.9V, 100mV/step, 13steps,
IMAX = 400mA, Input Power is BLDOIN
 - BLDO2: 0.7V~1.9V, 100mV/step, 13steps,
IMAX = 300mA, Input Power is BLDOIN
 - BLDO3: 0.7V~1.9V, 100mV/step, 13steps,
IMAX = 200mA, Input Power is BLDOIN
 - BLDO4: 0.7V~1.9V, 100mV/step, 13steps,
IMAX = 200mA, Input Power is BLDOIN
 - CLDO1: 0.7V~3.3V, 100mV/step, 27steps,
IMAX = 400mA, Input Power is CLDOIN
 - CLDO2: 0.7V~3.4V, 100mV/step, 28steps,
3.6~4.2V, 200mV/step, 4steps,
IMAX = 300mA, Input Power is CLDOIN
 - CLDO3: 0.7~3.3V, 100mV/step, 27steps,
IMAX = 200mA, Input Power is CLDOIN
- **Poly-Phase**
 - DCDC A&B: Dual-phase, IMAX = 5A
 - DCDC A&B&C: Tri-phase, IMAX = 7.5A
 - DCDC D&E: Dual-phase, IMAX = 3A
 - Other feature: switching frequency: 3MHz,
1.5uH/1uH, internal soft-starting, DCDC
A/C/D support DVM
- **10-CH LDO**
 - ALDO1: 0.7V~3.3V, 100mV/step, 27steps,
IMAX = 300mA, Input Power is ALDOIN
 - ALDO2: 0.7V~3.3V, 100mV/step, 27steps,
IMAX = 300mA, Input Power is ALDOIN
- Supports TWIS(Two Wire Serial Interface)
protocol, Address is 0x6C/0x6D
 - IRQ is an open drain output
 - Internal over temperature protection
 - Internal voltage monitor, monitors the output
voltage of DCDC A/B/C/D/E, internal outputs PWR
OK (open drain)signal
 - Power on-off key
 - On/Off: Typical value of on-resistance is 90 mΩ
 - Package: QFN 7x7, 56-pin
 - Applications
 - STB
 - OTT
 - Tablet
 - Smart phone
 - Computer

3. Typical Application

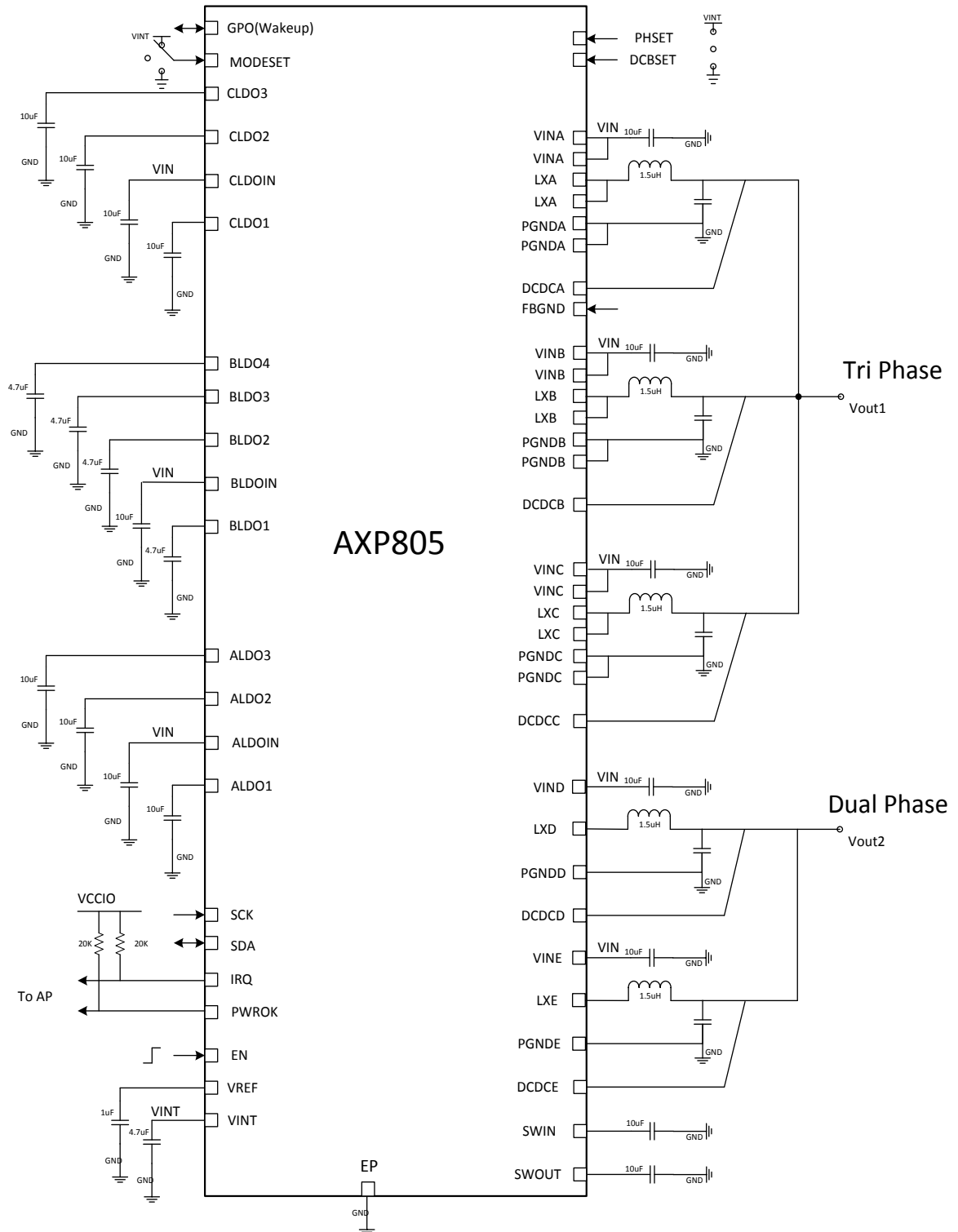


Figure 1. Typical Application

4. Block Diagram

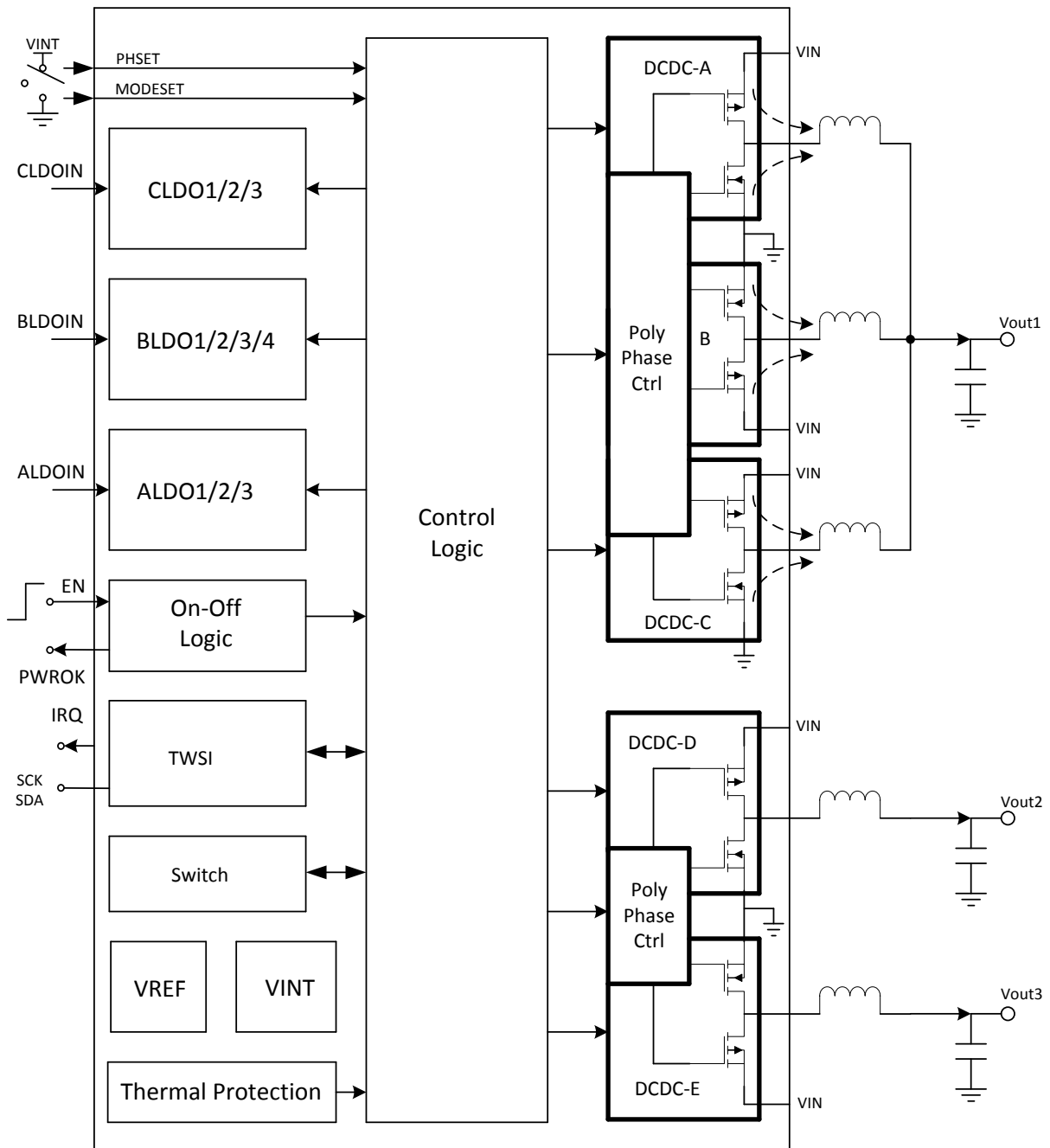


Figure 2. Block Diagram

5. Pin Description

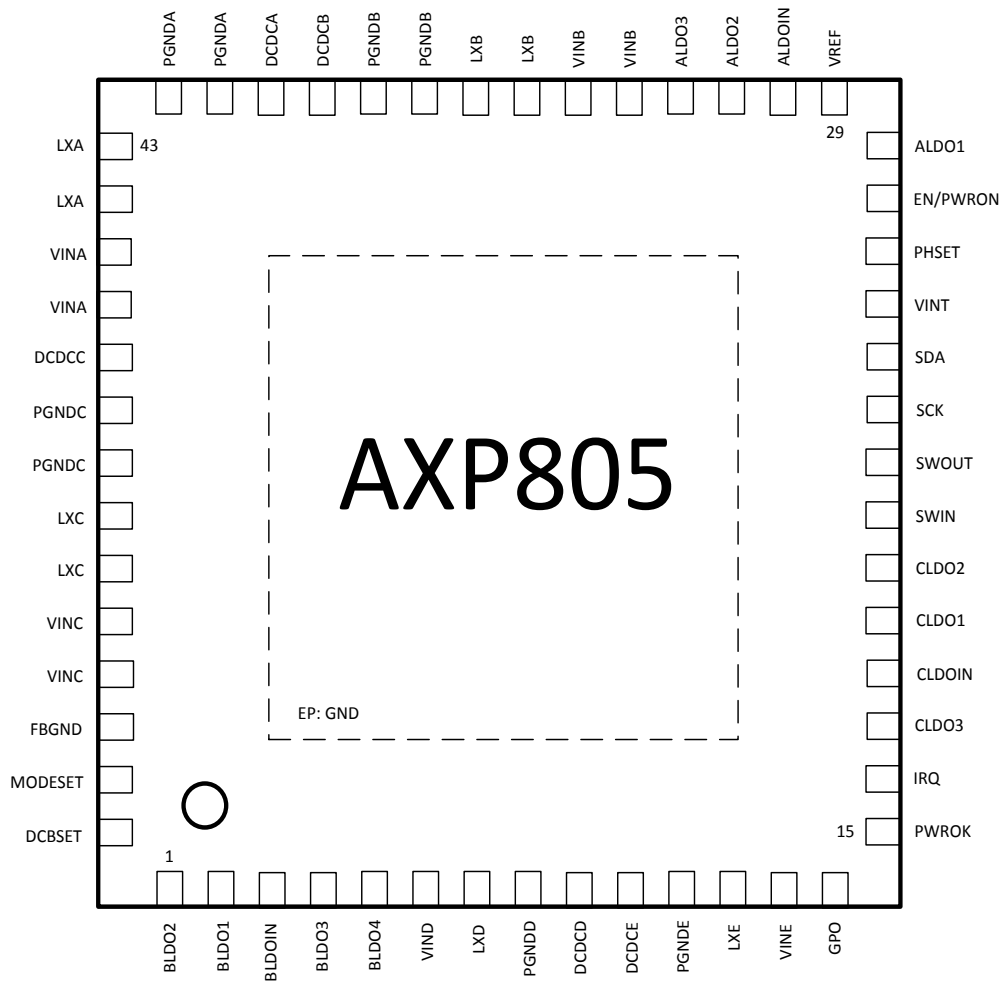


Figure 3. QFN-56

Table 1. Pin Description

NO.	Symbol	Type	Description
1	BLDO2	O	Output pin of BLDO2
2	BLDO1	O	Output pin of BLDO1
3	BLDOIN	PI	BLDOs input source
4	BLDO3	O	Output pin of BLDO3
5	BLDO4	O	Output pin of BLDO4
6	VIND	PI	DCDCD input source
7	LXD	IO	Inductor pin for DCDCD
8	PGNDD	G	NMOS GND for DCDCD

9	DCDCD	I	Feedback pin for DCDCD
10	DCDCE	I	Feedback pin for DCDCE
11	PGNDE	G	NMOS GND for DCDCE
12	LXE	IO	Inductor pin for DCDCE
13	VINE	PI	DCDCE input source
14	GPO	IO	GPO or Wakeup pin by REG35
15	PWROK	O	Power good indication output
16	IRQ	O	IRQ output
17	CLDO3	O	Output pin of CLDO3
18	CLDOIN	PI	CLDOs input source
19	CLDO1	O	Output pin of CLDO1
20	CLDO2	O	Output pin of CLDO2
21	SWIN	PI	Switch input source
22	SWOUT	O	Switch Output pin
23	SCK	I	Clock pin for serial interface. Connected to IO power by 2.2kohm resistor while use TWSI.
24	SDA	IO	Data pin for serial interface. Connected to IO power by 2.2kohm resistor while use TWSI.
25	VINT	O	Internal logic power, 1.8V
26	PHSET	I	Set DCDCA/B/C work mode (lonely/Dual-phase/Tri-phase)
27	EN	I	Enable pin for PMIC in master/slave mode. Or PWRON pin in self-work mode.
28	ALDO1	O	Output pin of ALDO1
29	VREF	O	Internal reference voltage
30	ALDOIN	PI	ALDOs input source
31	ALDO2	O	Output pin of ALDO2
32	ALDO3	O	Output pin of ALDO3
33	VINB	PI	DCDCB input source
34			
35	LXB	IO	Inductor pin for DCDCB
36			
37	PGNDB	G	NMOS GND for DCDCB
38			
39	DCDCB	I	Feedback pin for DCDCB
40	DCDCA	I	Feedback pin for DCDCA
41	PGNDA	G	NMOS GND for DCDCA
42			
43	LXA	IO	Inductor pin for DCDCA
44			
45	VINA	PI	DCDCA input source
46			
47	DCDCC	I	Feedback pin for DCDCC
48	PGNDC	G	NMOS GND for DCDCC
49			

50	LXC	IO	Inductor pin for DCDCC
51			
52	VINC	PI	DCDCC input source
53			
54	FBGND	I	Feedback minus pin for DCDCA
55	MODESET	I	Set work mode for PMIC. (GND: Slave mode; VINT: Master mode; Floating: Self-work mode)
56	DCBSET	I	Set default output voltage for DCDCA
57	EP	G	Exposed Pad, connected to system GND

6. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this standard may damage to the device.

Table 2. Absolute Maximum Ratings

Parameter	Description	Value	Unit
VIN	DCDCs/LDOs Input Voltage	-0.3 ~ 6.3	V
Tj	Operating Junction Temperature Range	<125	°C
Ta	Operating Ambient Temperature Range	-20 ~ 85	°C
Tstg	Storage Temperature Range	-40 ~150	°C
T _{LEAD}	Maximum Soldering Temperature (at leads, 10sec)	260	°C
V _{ESD}	Maximum ESD stress voltage, Human Body Model	>=2000	V
PD	Internal Power Dissipation	TBD	mW
θ _{JA}	Junction-to-Ambient Thermal Resistance	TBD	°C/W

7. Electrical Characteristics

Ta = 25°C (Unless otherwise stated)

Table 3. Electrical Characteristics

Symbol	Description	Conditions	Min	Type	Max	Units
VIN						
V _{IN}	Input Voltage		3.0		5.5	V
V _{UVLO}	VIN Under Voltage Lockout		2.6	2.6	3.3	V
Off Mode Current						
I _{BATOFF}	OFF Mode Current	BAT=3.7V		25		μA
Logic						
V _{IL}	Logic Low Input Voltage			0.3		V
V _{IH}	Logic High Input Voltage			1.2		V
TWSI						
V _{CC}	Input Supply Voltage		1.8	3.3		V
Addr	TWSI Slave Address (7 bits)		0x6C	0x6C	0x6D	
f _{SCK}	Clock Operating Frequency			400	1000	kHz
t _f	Clock Data Fall Time	2.2kΩ Pull High		60		ns
t _r	Clock Data Rise Time	2.2 kΩ Pull High		100		ns
RSB						
V _{CC}	Input Supply Voltage			1.8		V
Addr	RSB Slave Address		0x03A2	0x03A2	0x04E6	
f _{SCK}	Clock Operating Frequency			3000		kHz
DCDCs						
f _{OSC}	Oscillator Frequency	Default		3		MHz
DCDCA						
I _{VINA}	Input Current	PFM Mode I _{DCDCAOUT} = 0		50		μA
I _{LIMA}	PMOS Switch Current Limit			3000		mA
I _{DCDCAOUT}	Available Output Current	Single phase		2500		mA
		Dual phase (DCDCA&B)		5000		
		Tri phase (DCDCA&B&C)		7500		
V _{DCDCAOUT}	Output Voltage		0.6	0.9	1.52	V

V _{DCDCA_ACC}	Output Voltage Accuracy	V _{DCDCA_DEFAULT} = 0.9V I _{DCDCAOUT} = 300mA	0.873		0.927	V
DCDCB						
I _{VINB}	Input Current	PFM Mode, I _{DCDCBOUT} = 0		40		μA
I _{LIMB}	PMOS Switch Current Limit			3000		mA
I _{DCDCBOUT}	Available Output Current			2500		mA
V _{DCDCBOUT}	Output Voltage	DCBSET is floating	1	0.9	2.55	V
V _{DCDCB_ACC}	Output Voltage Accuracy	V _{DCDCB_DEFAULT} = 1.35V I _{DCDCBOUT} = 350mA	1.3095		1.3905	V
DCDCC						
I _{VINC}	Input Current	PFM Mode, I _{DCDCCOUT} = 0		40		μA
I _{LIMC}	PMOS Switch Current Limit			3000		mA
I _{DCDCCOUT}	Available Output Current			2500		mA
V _{DCDCCOUT}	Output Voltage		0.6	0.9	1.52	V
V _{DCDCC_ACC}	Output Voltage Accuracy	V _{DCDCC_DEFAULTT} = 0.9V I _{DCDCCOUT} = 300mA	0.873		0.927	V
DCDCD						
I _{VIND}	Input Current	PFM Mode, I _{DCDCDOUT} = 0		40		μA
I _{LIMD}	PMOS Switch Current Limit			2000		mA
I _{DCDCDOUT}	Available Output Current	Single phase		1500		mA
		Dual phase (DCDC D&E)		3000		
V _{DCDCDOUT}	Output Voltage		0.6	0.9	3.3	V
V _{DCDCD_ACC}	Output Voltage Accuracy	V _{DCDCD_DEFAULT} = 0.9V I _{DCDCDOUT} = 150mA	0.873		0.927	V
DCDCE						
I _{VINE}	Input Current	PFM Mode, I _{DCDCEOUT} = 0		50		μA
I _{LIME}	Switch Current Limit Per PMOS			2000		mA
I _{DCDCEOUT}	Available Output Current			1500		mA
V _{DCDCEOUT}	Output Voltage		1.1	1.2	3.4	V
V _{DCDCE_ACC}	Output Voltage Accuracy	V _{DCDCE_DEFAULT} = 1.2V I _{DCDCEOUT} = 200mA	1.164		1.236	V
ALDO1						
V _{ALDO1}	Output Voltage	I _{ALDO1} = 1mA	0.7	3.3	3.3	V
I _{ALDO1}	Output Current			300		mA
I _Q	Quiescent Current			50		μA

PSRR	Power Supply Rejection Ratio			TBD		dB
e _N	Output Noise,20Hz-80KHz	V _{ALDO1} =1.8V, I _{ALDO1} =10mA		40		μV _{RMS}
V _{ALDO1_ACC}	Output Voltage Accuracy	V _{ALDO1_DEFAULT} = 3.3V I _{ALDO1} = 66mA	3.201		3.399	V
ALDO2						
V _{ALDO2}	Output Voltage	I _{ALDO2} =1mA	0.7		3.3	V
I _{ALDO2}	Output Current			300		mA
I _Q	Quiescent Current			50		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
e _N	Output Noise,20Hz-80KHz	V _{ALDO2} =1.8V, I _{ALDO2} =10mA		40		μV _{RMS}
V _{ALDO2_ACC}	Output Voltage Accuracy	V _{ALDO2_DEFAULT} = 3V I _{ALDO2} = 60mA	2.91		3.09	V
ALDO3						
V _{ALDO3}	Output Voltage	I _{ALDO3} =1mA	0.7		3.3	V
I _{ALDO3}	Output Current			300		mA
I _Q	Quiescent Current			50		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
e _N	Output Noise,20Hz-80KHz	V _{ALDO3} =1.8V, I _{ALDO3} =10mA		40		μV _{RMS}
V _{ALDO3_ACC}	Output Voltage Accuracy	V _{ALDO3_DEFAULT} = 3V I _{ALDO3} = 60mA	2.91		3.09	V
BLDO1						
V _{BLDO1}	Output Voltage	I _{BLDO1} =1mA	0.7	1.8	1.9	V
I _{BLDO1}	Output Current			400		mA
I _Q	Quiescent Current			40		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
V _{BLDO1_ACC}	Output Voltage Accuracy	V _{BLDO1_DEFAULT} = 1.8V I _{BLDO1} = 60mA	1.746		1.854	V
BLDO2						
V _{BLDO2}	Output Voltage	I _{BLDO2} =1mA	0.7	1.8	1.9	V
I _{BLDO2}	Output Current			200		mA
I _Q	Quiescent Current			40		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
V _{BLDO2_ACC}	Output Voltage Accuracy	V _{BLDO2_DEFAULT} = 1.8V I _{BLDO2} = 60mA	1.746		1.854	V
BLDO3						
V _{BLDO3}	Output Voltage	I _{BLDO3} =1mA	0.7		1.9	V

I_{BLDO3}	Output Current			200		mA
I_Q	Quiescent Current			40		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
V_{BLDO3_ACC}	Output Voltage Accuracy	$V_{BLDO3_DEFAULT} = 1.5V$ $I_{BLDO3} = 50mA$	1.455		1.545	V
BLDO4						
V_{BLDO4}	Output Voltage	$I_{BLDO4}=1mA$	0.7		1.9	V
I_{BLDO4}	Output Current			100		mA
I_Q	Quiescent Current			40		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
V_{BLDO4_ACC}	Output Voltage Accuracy	$V_{BLDO4_DEFAULT} = 1.5V$ $I_{BLDO4} = 50mA$	1.455		1.545	V
CLDO1						
V_{CLDO1}	Output Voltage	$I_{CLDO1}=1mA$	0.7	3.3	3.3	V
I_{CLDO1}	Output Current			300		mA
I_Q	Quiescent Current			50		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
e_N	Output Noise,20Hz-80KHz	$V_{CLDO1}=1.8V$, $I_{CLDO1}=10mA$		40		μV_{RMS}
V_{CLDO1_ACC}	Output Voltage Accuracy	$V_{CLDO1_DEFAULT} = 3.3V$ $I_{CLDO1} = 66mA$	3.201		3.399	V
CLDO2						
V_{CLDO2}	Output Voltage	$I_{CLDO2}=1mA$	0.7		4.2	V
I_{CLDO2}	Output Current			300		mA
I_Q	Quiescent Current			50		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
e_N	Output Noise,20Hz-80KHz	$V_{CLDO2}=1.8V$, $I_{CLDO2}=10mA$		40		μV_{RMS}
V_{CLDO2_ACC}	Output Voltage Accuracy	$V_{CLDO2_DEFAULT} = 3.3V$ $I_{CLDO2} = 66mA$	3.201		3.399	V
CLDO3						
V_{CLDO3}	Output Voltage	$I_{CLDO3}=1mA$	0.7		3.3	V
I_{CLDO3}	Output Current			300		mA
I_Q	Quiescent Current			50		μA
PSRR	Power Supply Rejection Ratio			TBD		dB
e_N	Output Noise,20Hz-80KHz	$V_{CLDO3}=1.8V$, $I_{CLDO3}=10mA$		40		μV_{RMS}
V_{CLDO3_ACC}	Output Voltage Accuracy	$V_{CLDO3_DEFAULT} = 3V$ $I_{CLDO3} = 60mA$	2.91	3	3.09	V

Switch						
Ron	Internal Ideal Resistance	Pin to Pin		90	100	mΩ

8. Control and Operation

PMIC has two status: power off and power on. Under the power off status, If all the output are closed (except VINT), The total power consumption is about 25uA. Under the power on status, all the output are active and Serial Interface (TWSI or RSB) work normally. We can change the status of each output. The total power consumption is about 400uA under no-load conditions.

In order to satisfy different application requirements, the default output voltage of 5-CH DCDCs, ALDO1, BLDO1/2, CLDO1 and start-up sequence can be customized. Other LDOs and SWs don't start up by default. PMIC monitors the output of the 5-CH DCDCs, and provides over-voltage/under-voltage protection.

PMIC has a switch and the typical value of internal resistance is 90mΩ. Typical application: DCDC provides 3.3V, and power supply for LCD Bias via the switch.

PMIC has a MODESET pin, which is used to set operating mode. (Master/Slave/Self-Work mode)

The functions of the three mode are as follows:

modeset pin	Mode	EN/PWRON	Internal VREF	Extended Address bit[0]	PWROK operating mode			
					pull down method	Detection of PWROK pin when starting up	pull down to restart (default)	4ms delay for normal shutdown
VINT	master	EN	ON	0	Pull down when shutdown	N	N	N
GND	slave	EN	OFF	1	Pull down when abnormal	N	N	N
floating	self-work	PWRON	ON	0	Pull down when shutdown	Y	Y	Y

NOTE:

- Under the Slave mode, VREF can turn off and accept the external input.
- Pull down when shutdown: During the process of starting up or shutting down, pull down the PWROK pin, and at other conditions, keep it floating.
Pull down when abnormal: The PMIC will not pull down PWROK but keep it floating. It will pull down the PWROK only in the case of power off, which caused by abnormal situations (It is not recovered until EN goes to low level or PMIC restarts).
- 4ms delays refers to the time delay between pulling down PWROK pin and closing output power in the power off sequence.(via REG1F[2] enable).
- Extended address: it is used for communication interface. Please refer to the Serial Interface.

When the PMIC is power on, VINT is opened firstly. After 8ms delay, it will judge the operating mode (power on reset) according to the status of MODESET pin, and store the result in REG00[7:6]. After judgement is completed, the VREF's work status is set according to the operating mode, and then PMIC judges whether it is power on.

8.1. Master mode

Under the power off status, PWROK remains being pulled down. If the voltage of EN pin goes from low to high level (When the voltage is higher than 0.6V, it is judged to be high level), Then the PMIC will power on, and each power outputs according to the timing which is set by factory. When the power output is completed, then after 64ms delay, the PWROK is released from being pulled down. After power on, the register value can be configure by serial interface.

In the normal condition, After each output is enabled, the power supply can be quickly powered on. If each power does not powered on within 32ms, it indicates the output load is abnormal. The PMIC will pull down the PWROK, and clear the boot signal automatically, and then wait for the next power on.

At the boot time, AXP805 can detect the status of the PWROK pin to determine whether the power is normal. If PWROK pin is not pulled up within 128ms after each output is active, it indicates the PMIC can not start up normally. PMIC will clear the boot signal automatically and wait for the next power on. Under the Master mode, this function is turned off by default and turned on by REG32[5].

After power on completed, PWROK will pull up by external. If external keys or other reasons pull down PWROK, PMIC does not respond to this case, and the PMIC will not restart. Under the Master Mode, Restarting the PMIC can only be achieved by writing '1' to the control register REG32[6].

Under the power on status, the power off sources are shown as the following.

- The voltage of EN pin goes from low to high level.
- Writing '1' to REG32[7]/REG3F[7].
- ALDOINGOOD goes from high to low level (ALDOIN < V_{OFF} (Default Value is 2.6V) or ALDOIN > 5.8V).
- The output voltage of DCDC A/B/C/D/E are lower than 85% of the setting voltage. (REG1D[7:3] determines whether to open).
- Internal over temperature, more than warning level (135°C, REG32[1] determines whether to open).

When any of the above cases occur, the shutdown process of PMIC will start to turn off each output (the sequence is determined by REG32[3]). After each output is off, Whether performing the internal discharge depends on REG1F[3].

NOTE:

- Above 1&2 cases are normal power off sources. The PMIC will pull down the PWROK pin and turn off each output. In default status, there is no delay between pulling down the PWROK pin and turning off each output (the 4ms delay can be opened by REG1F[2]).
- Above 3~5 cases are abnormal power off sources. The PMIC will pull down the PWROK pin firstly and turn off the power output after delaying for 4ms.

8.2. Slave mode

Under the power off status, PWROK remains floating. If the voltage of EN pin goes from low to high level (When the voltage is higher than 0.6V, it is judged to be high level.) Then the PMIC will power on, and each power outputs according to the sequence, which is factory settings. If there is no abnormal situation of the power supply, PWROK keeps floating throughout the process.

In the normal condition, power supply can be quickly powered on After each output enable signal is active. If each power does not powered on within 32ms, it indicates the output load is abnormal. The PMIC will pull down the PWROK, and clear the boot signal automatically, and then wait for the next power on.

At the boot time, AXP805 can detect the status of the PWROK pin to determine whether the power is normal. If PWROK pin is not pulled up within 128ms after each output is active, it indicates the PMIC can not

start up normally. PMIC will clear the boot signal automatically, and wait for the next power on. Under the Slave mode, this function is turned off by default and turned on by REG32[5].

After power on completed, PWROK will pulled on by external. If external keys or other reasons pull down PWROK, PMIC does not respond to this case, and the PMIC will not restart. Under the Slave Mode, restart the PMIC can only be achieved by writing '1' to the control register REG32[6].

Under the power on status, the power off sources are shown as the following.

- The voltage of EN pin goes from low to high level.
- Writing '1' to REG32[7]/REG3F[7].
- ALDOINGOOD goes from high to low level($ALDOIN < V_{OFF}$ (Default Value is 2.6V) or $ALDOIN > 5.8V$).
- The output voltage of DCDC A/B/C/D/E are lower than 85% of the setting voltage.(REG1D[7:3] determines whether to open or not).
- Internal over-temperature, more than warning level($135^{\circ}C$, REG32[1] determines whether or not to open).

When any of the above cases occur, the shutdown process of PMIC will start to turn off each output(the sequence is determined by REG32[3]). Whether performing the internal discharge depends on REG1F[3].

NOTE:

- Above 1&2 cases are normal power off sources. The PMIC will not pull down the PWROK pin and turn off each output. In default status, there is no delay between pulling down the PWROK pin and turning off each output (the 4ms delay can be opened by REG1F[2]).
- Above 3~5 cases are abnormal power off sources. The PMIC will pull down the PWROK pin firstly and turn off the output after delaying for 4ms.

8.3. Self-work mode

Under the Self-Work Mode, the function of EN/PWRON pin is PWRON which is internally pulled up to VINT. A power on-off Key(POK) can be connected between PWRON pin and GND.

Under the power off status, PWROK remains being pulled down. There are the following cases:

- The time of pulling down POK is more than ONLEVEL.
- ALDOINGOOD goes from low to high level (which can be customized to be enabled).
- If REG1F[7]=1, and IRQ is low level and passes through the internal 16ms de-bounce.

If any of above cases occur, PMIC will be power on, and each power starts output according to the sequence, which is factory settings. When each power output is finished, after delaying for 64ms, the PWROK is released from being pulled down, so the entire boot process is complete. After that, the register values can be changed by the serial interface.

In the normal conditions, the power supply can be quickly powered on after each output enable signal is active. If each power does not powered on within 32ms, it indicates the output load is abnormal. PMIC will pull down PWROK, and clear boot signal automatically, and then wait for the next power on.

At the boot time, the PMIC can detect the status of the PWROK pin to determine whether the power is normal. If PWROK pin is not pulled up within 128ms after each output is active, it indicates the PMIC can not start up normally. PMIC will clear the boot signal automatically, wait for the next power on. Under the Self-Work mode, this function is turned on by default.

After power on completed, external will pull on PWROK. If external keys or other reasons pull down PWROK, the PMIC will judge system exceptions and restart. Under the Self-Work Mode, restart the PMIC can also be achieved by writing '1' to the control register REG32[6].

NOTE:

- Under the Self-Work Mode, when the PMIC restarts, after each output of PMIC is enabled, the PMIC will detect the PWROK pin within 6s(Not 128ms) to judge whether it is pulled up successfully. If PWROK is pulled up, the restart process is over, otherwise, PMIC will shut down automatically. (If PWROK is pulled down because external power is abnormal, PMIC will be shutdown automatically. To avoid the long time of reset by POK, the time is set to be 6s.).
- The function of pulling down PWROK to restart is turned off by default, and it is opened by REG32[4].

Under the power on status, the power off sources are shown as the following.

- The time of pulling down PWRON button is more than ONLEVEL (determined whether this function is open by REG36[3], and it is determined by REG36[2] whether to start automatically or not after this function is turned off.)
- Writing “1” to the REG32[7]/REG3F[7].
- ALDOINGOOD goes from high to low level($ALDOIN < V_{OFF}$ (default is 2.9V), or $ALDOIN > 5.8V$).
- The output voltage of DCDC A/B/C/D/E are lower than 85% of the setting voltage(it is determined whether or not to open by REG1D[7:3]).
- PMIC Internal temperature exceeds warning level 2(125°C, REG32[1] determines whether or not to open).

When any of above cases occur, the shutdown process of PMIC will start to turn off each output (the sequence is determined by REG32[3]). After that, REG1F[3] decide whether to discharge internally.

NOTE:

- Above 1&2 cases are normal power off sources. The PMIC will pull down the PWROK pin firstly and turn off each output after delaying for 4ms (the 4ms delay can be opened by REG1F[2]). In default status, there is no delay between pulling down the PWROK pin and turning off each output (the function of delaying for 4ms can be closed by REG1F[2]).
- Above 3~5 cases are abnormal power off sources. The PMIC will pull down the PWROK pin firstly and turn off the power output after delaying for 4ms.

Under the power on status, POK has the following functions:

- If the pulse width of POK is greater than the internal 32ms de-bounce, and less than IRQLEVEL, PMIC will send POKSIRQ.
- If the pulse width of POK is greater than IRQLEVEL, PMIC will send POKLIRQ.
- If the pulse width of POK is greater than 16s, PMIC will force shutdown. After that, and delay for 64ms, there will power on reset and detect the boot source. (This function is controlled by REG32[0], which is turned off by default).

8.4. Sleep and Wakeup

PMIC has a GPIO pin, its function is set by REG35, which can be used for input/output of Wakeup signal. When this pin is used for input, PMIC will wake up by receiving the Wakeup signal under the Standby status. At this time, internal de-bounce is set for 1ms; When this pin is used for output, In order to wake up the PMIC, the GPIO pin need to send Wakeup signal and wait for 1s, and then execute the internal wakeup circuit.

Under the power on status, the system's Standby & Wakeup have the following two methods:

Method 1: PMIC plays a major role, and CPU controls a little

- REG31_[3] is set to 1, which is controlled by CPU. Before that, PMIC saves the state of each output
- System saves the state, and adjusts the PMIC output

- When working with multiple POWER ICs, you may come across some situations where you need to turn off different ICs' power at the same time. At this point, the processing are the following steps:
 - Write "1" to 0x1F[6] of each IC, and write the target value of REG10/11 to the corresponding buffer register.
 - Write "1" to 0x3F[6] using the broadcast address, Each IC exports the value from buffer register to REG10/11, and clears the flag automatically. (Please refer to the [serial interface](#))
- There are the following cases:
 - REG31[5]/REG3F[5] are set to 1(Multiple ICs wake up at the same time, and REG3F[5] must be set)
 - POKNIRQ/POKLIRQ (Self-Work Mode, the corresponding active level of IRQ Enable is high)
 - REG1F[7]=1, IRQ is low level and passes the 16ms de-bounce
 - Wakeup pin received the high or low level. (This pin is configured as Wakeup IN)

When any of above cases occur, REG10/11 recover to the state, that before REG31_[3] is written to 1. Each output voltage recovers to default value, which is determined by REG31_[6].
- **NOTE:**
 - **After REG31_[3] is set to 1, there is a 8ms protection period, and PMIC will not wakeup at this time.**
 - **When the output voltage recovers to the default value, please note that the default value of DCDC-B are determined by DCBSET pin and customization.**
- After the completion of each output recovery, REG31_[3], REG31_[5] and REG3F[5] are cleared automatically. After that, PWROK whether to drive low firstly and then go high depending on REG31_[7].

Method 2: It is controlled by CPUS, and it is irrelevant to REG31.

- After satisfying the super standby's condition, CPUS firstly remembers the power which needs to be turned off and its voltage value. After that, CPUS closes the relative power.
- System enters the super standby state
- CPUS judge whether to wakeup according to the system state
- According to the previous memory, CPUS fills the voltage register and on-off register of each power one by one, which need to be opened.
- Each output of PMIC wakeup
- After sufficient delay, CPUS thinks that power recovers normally, and releases the reset of CPU, and system begins to recover.

Add REG1A[3] to control whether to open DVM function of DCDC A/C/D when the PMIC wakeup. When bit3 and bit0/1/2 are set to '1' at the same time and the PMIC wakeup, corresponding DCDC has the function of DVM.

8.5. Reference、Internal Power and Interrupt

AXP805 has a VINT pin, which works as a LDO output with 1.8V and powers for the logic circuit. This pin requires an external 4.7uF capacitor, and IMAX > 100mA.

AXP805 has an IRQ pin, and the output is OD, which is connected to the NMI of master device. When the AXP805 detects the key, over-temperature and under-voltage and so on, and corresponding IRQ is enabled, IRQ pin will be pulled down to notice master device. When REG1F[7] is set to '1', The internal of IRQ provides a weak pull-up of around 20uA. If the IRQ pin is pulled-down externally and passes the internal de-bounce, the PMIC will be powered on automatically.

The VREF of PMIC can accept external input. When the PMIC is in Mater/Self-Work Mode, it will use the internal VREF. When the PMIC is in Slave Mode, it will use the external VREF and close the internal VREF.

8.6. Multi-Power Outputs

AXP805 provides 5-CH DCDCs, 10-CH LDOs and 1-CH Switch output. DCDC1~5 are automatically switchable between PFM and PWM by default. Its switching frequency is 3MHz. Under the typical condition, its inductor is 1.5uH, and output capacitor is 10uF. The voltage range and the driving ability of each output are shown in the following table.

Table 4. The output voltage and driving ability

Rails	Enable Bit	Voltage Register	Output Range	Default Voltage	Sequence	Max Load
DCDCA	REG10H[0]	REG12H	0.6V~1.52V	0.9V	2	2.5A
DCDCB	REG10H[1]	REG13H	1.0V~2.55V	0.9V	2	2.5A
DCDCC	REG10H[2]	REG14H	0.6V~1.52V	0.9V	2	2.5A
DCDCD	REG10H[3]	REG15H	0.6V~3.3V	0.9V	1	1.5A
DCDCE	REG10H[4]	REG16H	1.1V~3.4V	1.2V	2	1.5A
ALDO1	REG10H[5]	REG17H	0.7V~3.3V	3.3V	2	0.3A
ALDO2	REG10H[6]	REG18H	0.7V~3.3V	/	OFF	0.3A
ALDO3	REG10H[7]	REG19H	0.7V~3.3V	/	OFF	0.3A
BLDO1	REG11H[0]	REG20H	0.7V~1.9V	1.8V	2	0.4A
BLDO2	REG11H[1]	REG21H	0.7V~1.9V	1.8V	2	0.3A
BLDO3	REG11H[2]	REG22H	0.7V~1.9V	/	OFF	0.2A
BLDO4	REG11H[3]	REG23H	0.7V~1.9V	/	OFF	0.2A
CLDO1	REG11H[4]	REG24H	0.7V~3.3V	3.3V	2	0.4A
CLDO2	REG11H[5]	REG25H	0.7V~4.2V	/	OFF	0.3A
CLDO3	REG11H[6]	REG26H	0.7V~3.3V	/	OFF	0.2A
Switch	REG11H[7]	/	/	/	OFF	/

DCDC A&B support Dual-Phase mode, and their Maximum load capacity is 5A. DCDC A&B&C support Tri-Phase mode, and their Maximum load capacity is 7.5A. PMIC detects the PHSET pin's status at boot time, and saves the status into REG1B[7:6]. After the boot is complete, the value of REG1B[7] can be changed by the Serial Interface to change the operating mode.

PHSET pin status	GND	VINT	Floating
A/B/C: operating mode	A/B/C work independently	A&B Poly-Phase	A&B&C Poly-Phase
REG1B[7:6]: corresponding value	00	01	10

DCDC D&E also support Dual-Phase mode, and their Maximum load capacity is 3A. The function that whether it is turned on by default can be customized, which can be controlled by REG1B[5]

NOTE: When poly-phase is open, only need to change the corresponding register of DCDCA or DCDCD to change the output state.

DCDC A/C/D support DVM. When the output voltage changes, REG1A can control the change slope.

DCDCA and FBGND are feedback of DCDC A, which are used to set the output voltage. DCDCA pin connects

to the load point, and FGBND pin connects to the ground of the load. The internal resistance of the PCB trace and the bonding line can be compensated, so that the voltage on both ends of load is accurate. When power on, the PMIC determines whether to open the compensation by judging whether the FGBND connects to the GND. If not compensated, FBGND floating will be used.

All the DCDC and LDO have a function of current limiting protection. When the current of load is greater than the current-limiting value, the output voltage will decrease. PMIC will real-time monitor the output voltage of DCDC A/B/C/D/E. When the output voltage is below a certain proportion of the target voltage, the PMIC will boot shutdown process (Whether shutdown depends on the corresponding REG1D.)

The auto-detection function of DCDC inductor: If the PMIC detects that the DCDC is not connected to the inductor, it will not boot the DCDC, and mask the output monitor.

The PMIC has a DCBSET pin, which is used to set the output voltage for default. When the DCBSET is connected to the VINT, the default output is 1.5V. When the DCBSET is connected to the GND, the default output is 1.2V. When DCBSET is floating, the default output of voltage can be customized, which is factory settings.

DCBSET	GND	VINT	floating
DCDCB, Default Voltage	1.2V	1.5V	customized, Default is 1.1V

8.7. Serial Interface

PMIC supports two communication protocols (the protocols is determined by REG3E, and the default protocol can be customized):

- TWSI, Address: 0x6C, 0x6D.
- RSB, Address: 0x03A2, 0x04E6.

When multiple AXP805 work with together, the communication protocol has the following points:

- Multiple power ICs use the same communication address, such as 0x6C/0x6D, and hang on the same bus.
- The high 4bits of 0xFE are the extension bits of the PMIC (its value can be customized and determined by MODESET, the extra bits are 0 directly). The extended address of multiple ICs are different with each other.
- When the high 4bits of 0xFF are same as the 0xFE, the PMIC will response, and you can read or write, otherwise the PMIC will not respond.
- 0xFF is special: When the communication address is right, you can write the value to 0xFE, regardless of whether 0xFF is match for the 0xFE. When you read the 0xFF, the PMIC will not response only as 0xFF is match for 0xFE.
- When communicating, write the value of 0xFE of the target communication PMIC to the high 4bits of 0xFF.
- Write the different value to the high 4bits of 0xFF, the communication can be switched between different PMIC on the bus.
- If the high 4bits are set to full 1(broadcast address), no matter what the value of 0xFE is, all the PMICs will response, and all the PMICs can be written at once(unreadable).

NOTE: In practical applications, this broadcast address is usually used only when different PMICs need to be coordinated, and only special registers (such as 0x3F) are written.

- The above changes do not need to change the operating mode of the protocol host, and the existing TWSI/RSB host can be used. When the extended addressing of 0xFE is set to 0x0 at the high 4bits (master/self-work mode), and the communication process is same as the original protocol, and there is no need to set the high 4bits of 0xFF.

9. Register

9.1. Register List

ADDR	Description	R/W	Default
REG00	Startup source	R	
REG03	Chip ID	R	/
REG04-07	4 data buffers	RW	00H
REG10	On-off ctrl 1	RW	3FH
REG11	On-off ctrl 2	RW	11H
REG12	DCDC-A voltage control	RW	32H
REG13	DCDC-B Voltage control	RW	02H
REG14	DCDC-C voltage control	RW	37H
REG15	DCDC-D voltage control	RW	1EH
REG16	DCDC-E Voltage control	RW	16H
REG17	ALDO1 voltage control	RW	1AH
REG18	ALDO2 voltage control	RW	00H
REG19	ALDO3 voltage control	RW	00H
REG1A	DCDC mode control1	RW	00H
REG1B	DCDC mode control2	RW	
REG1C	DCDC frequency setting	RW	08H
REG1D	output monitor control	RW	FDH
REG1F	IRQ & PWROK & Off discharge setting	RW	
REG20	BLDO1 voltage control	RW	0BH
REG21	BLDO2 voltage control	RW	
REG22	BLDO3 voltage control	RW	00H
REG23	BLDO4 voltage control	RW	00H
REG24	CLDO1 voltage control	RW	1AH
REG25	CLDO2 voltage control	RW	00H
REG26	CLDO3 voltage control	RW	00H
REG31	power wakeup ctrl & VOFF setting	RW	00H
REG32	power disable & power down sequence	RW	
REG35	Wakeup pin function setting	RW	00H
REG36	POK setting	RW	59H
REG3E	Interface mode select	RW	00H
REG3F	Special control register	RW	00H
REG40	IRQ enable1	RW	03H
REG41	IRQ enable2	RW	03H
REG48	IRQ status1	RW	00H
REG49	IRQ status2	RW	00H
REGF3	VREF & Temperature warning level setting	RW	01H
REGFE	Serial interface address extension	RW	00H
REGFF	Register address extension	RW	00H

The register has two kinds of reset signals:

System reset means that the registers will be reset when the PMIC is power on.

Power on reset means that the registers will be reset when the PMIC is powered up.

9.2. Register Description

9.2.1. REG 00: Startup Source

Reset: system reset

Bit	Description	R/W
7-6	Chip Mode 00:Slave 11:Master 10:Self-Work 01:Reserved	R
5	Startup by ALDOINGOOD from low to high when EN is high	R
4	Startup by EN from low to high when ALDOINGOOD is high	R
3	Startup by IRQ pin	R
2	Startup by PWRON press	R
1	Startup by PWRON special sequence	R
0	Startup by ALDOIN from low to high	R

NOTE:

- If restart, there is no flag
- If multiple boot sources arrive at the same time, they are all set to high.

9.2.2. REG 03: IC Type NO.

Bit	Description	R/W
5-4	IC Version NO.	R
7-6 & 3-0	IC Type NO. 010000: IC is AXP805 Others: Reserved	R

9.2.3. REG 04-07: 4 Data Buffers

Reset: power on reset

9.2.4. REG 10: Output Power on-off Control 1

Default: 3FH

Reset: system reset

Bit	Description	R/W	Default
7	ALDO3 on-off control	RW	0
6	ALDO2 on-off control	RW	0
5	ALDO1 on-off control	RW	1
4	DCDC-E on-off control	RW	1
3	DCDC-D on-off control	RW	1
2	DCDC-C on-off control	RW	1
1	DCDC-B on-off control	RW	1

0	DCDC-A on-off control	RW	1
---	-----------------------	----	---

NOTE: The internal PMIC designs a buffer register for REG10. When REG1F[6] is set to 0, the address of 0x10H will point to REG10. When REG1F[6] is set to 1, it will export the REG10's value to its buffer register, and the address of 0x10H points to the buffer register, and REG10's value has no change. When REG3F[6] is set to 1, it will export the buffer register's value to REG10. After that, it will set REG1F[6] and REG3F[6] to 0, and the address of 0x10H points to REG10.

9.2.5. REG 11: Output Power on-off Control 2

Default: 11H

Reset: system reset

Bit	Description	R/W	Default
7	SW on-off control	RW	0
6	CLDO3 on-off control	RW	0
5	CLDO2 on-off control	RW	0
4	CLDO1 on-off control	RW	1
3	BLDO4 on-off control	RW	0
2	BLDO3 on-off control	RW	0
1	BLDO2 on-off control	RW	0
0	BLDO1 on-off control	RW	1

NOTE: The internal PMIC designs a buffer register for REG11. When REG1F[6] is set to 0, the address of 0x11H will point to REG11. When REG1F[6] is set to 1, it will export the REG11's value to its buffer register, and the address of 0x11H points to buffer register, and REG11's value has no change. When REG3F[6] is set to 1, it will export the buffer register's value to REG11. After that, it will set REG1F[6] and REG3F[6] to 0, and the address of 0x11H points to REG11.

9.2.6. REG 12: DCDC-A Voltage Control

Default: 32H

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-A voltage setting bit5-0: 0.6V~1.1V, 10mV/step, 51steps 1.12V~1.52V, 20mV/step, 21steps	RW	0110010

9.2.7. REG 13: DCDC-B Voltage Control

Default: 02H

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	DCDC-B voltage setting bit4-0: 1.0V~2.55V, 50mV/step, 32steps	RW	00010

NOTE:

- The default value is determined by DCBSET according to the application.
- When DCBSET is connected to the VINT, the default output is 1.5V; When the DCBSET is connected the

GND, the default output is 1.2V. When DCBSET is floating, the default output of voltage can be customized.

- The range of customization: 1.0V~2.55V.

9.2.8. REG 14: DCDC-C Voltage Control

Default: 37H

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-C voltage setting bit6-0: 0.6V~1.1V, 10mV/step, 51steps 1.12V~1.52V, 20mV/step, 21steps	RW	110111

9.2.9. REG 15: DCDC-D Voltage Control

Default: 1EH

Reset: system reset

Bit	Description	R/W	Default
7-6	Reserved	RW	00
5-0	DCDC-D voltage setting bit5-0: 0.6~1.5V, 20mV/step, 46steps 1.6~3.3V, 100mV/step, 18steps	RW	11110

9.2.10. REG 16: DCDC-E Voltage Control

Default: 16H

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	DCDC-E voltage setting bit4-0: 1.1~3.4V, 100mV/step, 24steps	RW	10110

9.2.11. REG 17: ALDO1 Voltage Control

Default: 1AH

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	ALDO1 voltage setting bit4-0: 0.7~3.3V, 100mV/step, 27steps	RW	11010

9.2.12. REG 18: ALDO2 Voltage Control

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	ALDO2 voltage setting bit4-0: 0.7~3.4V, 100mV/step, 27steps	RW	00000

9.2.13. REG 19: ALDO3 Voltage Control

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	ALDO3 voltage setting bit4-0: 0.7~3.3V, 100mV/step, 27steps	RW	00000

9.2.14. REG 1A: DCDC Mode Control 1

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6	DCDC-D DVM voltage ramp control	0: 1step/15.625us 1: 1step/31.250us	0
5	DCDC-C DVM voltage ramp control		0
4	DCDC-A DVM voltage ramp control		0
3	DVM on-off control when wakeup	0: Disable 1: Enable	0
2	DCDC-D DVM on-off control	0: Disable 1: Enable	0
1	DCDC-C DVM on-off control		0
0	DCDC-A DVM on-off control		0

9.2.15. REG 1B: DCDC Mode Control 2

Default: UDF

Reset: system reset

Bit	Description	R/W	Default
7-6	DCDC A&B&C poly-phase control 00: No poly-phase 01: A&B Dual-phase 10: A&B&C Tri-phase 11: No poly-phase	RW	PHSET
5	DCDC D&E poly-phase control 0: No poly-phase 1: Poly-phase	RW	x
4-0	Reserved	RW	0

NOTE: The PMIC starts to import the status of PHSET into bit[7:6], and then, bit[7:6] is controlled by the serial interface. The default of bit[5] is determined by the actual application.

9.2.16. REG 1C: DCDC Frequency Setting

Default: 08H

Reset: system reset

Bit	Description	R/W	Default
7	DCDC frequency spread enable 0: Disable	RW	0

	1: Enable		
6	DCDC frequency spread range control 0: 50KHz 1: 100KHz	RW	0
5-0	Reserved	RW	001000

9.2.17. REG 1D: Output Monitor Control

Default: FDH

Reset: Power on reset

Bit	Description	R/W	Default
7	DCDC-E 85% low voltage turn off PMIC function 0: Disable 1: Enable	RW	1
6	DCDC-D 85% low voltage turn off PMIC function 0: Disable 1: Enable	RW	1
5	DCDC-C 85% low voltage turn off PMIC function 0: Disable 1: Enable	RW	1
4	DCDC-B 85% low voltage turn off PMIC function 0: Disable 1: Enable	RW	1
3	DCDC-A 85% low voltage turn off PMIC function 0: Disable 1: Enable	RW	1
2	Reserved	RW	1
1-0	DCDC A/B/C output voltage monitor de-bounce time setting 00: 62us 01: 124us 10: 186us 11: 248us	RW	01

9.2.18. REG 1F: IRQ & PWROK & Off Discharge Setting

Default: UDF (Determined by the actual application), Mode indicates that it is determined by the operating mode of IC.

Reset: Power on reset, bit6 为 System reset

Bit	Description	R/W	Default
7	IRQ pin turn on or wakeup AXP805 function enable when IC is Self-Work Mode; IRQ pin wakeup AXP805 function enable when IC is Master/Slave Mode. 0: Disable 1: Enable	RW	0
6	Register address 0x10/0x11 destination register control 0: REG10/11 1: REG10/11 corresponding buffer register The following cases also need to clear the bit:	RW	0

	1). When Wakeup occurs, there need not to export the buffer register to REG10/11, that can be cleared. 2). When the 3F[6] is set to 1, there need to export the buffer register to REG10/11, and then clear it.		
5	Reserved	RW	0
4	Reserved	RW	0
3	Internal off-discharge for DCDC&LDO 0: Disable 1: Enable	RW	1
2	PMIC normal power-off 4ms delay enable 0: Disable 1: Enable Default: 0 in Master/Slave Mode 1 in Self-Work Mode NOTE: In the slave mode, it refers to the delay between the internal shutdown signal and closing each output. In the master/self-work mode, it refers to the delay between pulling down PWROK and closing each output	RW	Mode
1-0	Delay time between PWROK signal and power good time 00: 8ms 01: 16ms 10: 32ms 11: 64ms Default: 10 in Slave Mode 11 in Master/Self-Work Mode	RW	Mode

9.2.19. REG 20: BLDO1 Voltage Control

Default: 0BH

Reset: system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3-0	BLDO1 voltage setting bit4-0: 0.7~1.9V, 100mV/step, 13steps	RW	1011

9.2.20. REG 21: BLDO2 Voltage Control

Default: UDF (Determined by actual application)

Reset: system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3-0	BLDO2 voltage setting bit3-0: 0.7~1.9V,100mV/step,13steps	RW	x

9.2.21. REG 22: BLDO3 Voltage Control

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3-0	BLDO3 voltage setting bit3-0: 0.7~1.9V,100mV/step,13steps	RW	0000

9.2.22. REG 23: BLDO4 Voltage Control

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3-0	BLDO4 voltage setting bit3-0: 0.7~1.9V,100mV/step,13steps	RW	0000

9.2.23. REG 24: CLDO1 Voltage Control

Default: 1AH

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	CLDO1 voltage setting bit4-0: 0.7~3.3V, 100mV/step, 27steps	RW	11010

9.2.24. REG 25: CLDO2 Voltage Control

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	CLDO2 voltage setting bit4-0: 0.7~3.4V,100mV/step,28steps 3.6~4.2V,200mV/step,4steps	RW	0 0000

9.2.25. REG 26: CLDO3 Voltage Control

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4-0	CLDO3 voltage setting bit4-0: 0.7~3.3V, 100mV/step, 27steps	RW	0 0000

9.2.26. REG 31: Power Wakeup Ctrl & VOFF Setting

Default: 00H

Reset: bit[3] is System reset, the others is Power on reset

Bit	Description	R/W	Default
7	PWROK drive low or not when Power wake up and REG31[3]=1 0: Not drive low 1: Drive low in wake up period	RW	0

6	Voltage recovery control when AXP805 wakeup (Valid only for the default output that can be customized) 0: Recovery to the default 1: Remain the same	RW	0
5	Soft Power wakeup, write 1 to this bit, the output power will be waken up, and this bit will clear itself	RW	0
4	Control bit for IRQ output and wake up trigger when REG31[3] is 1 0 : IRQ pin is masked and IRQ can wake up AXP805 1 : IRQ pin is normal and IRQ cannot wake up AXP805	RW	0
3	Enable bit for the function that output power be waken up by REG31_[5], POKNIRQ, POKLIRQ or IRQ pin is Low.	RW	0
2-0	V _{OFF} setting bit2-0: 2.6~3.3V, 0.1V/step, 8steps	RW	000

9.2.27. REG 32: Power Disable & Power Down Sequence

Default: UDF, Mode: indicated that it is determined by the operating mode of IC.

Reset: bit [7:6] is system reset, the others is Power on reset

Bit	Description	R/W	Default
7	Power disable control. Write '1' to this bit will power off the PMIC, and this bit will clear itself	RW	0
6	Host restart the PMIC and clear itself	RW	0
5	Monitor PWROK pin status, and detect power-on normal or not 0: Disable 1: Enable Default: 0 in Master/Slave Mode 1 in Self-Work Mode	RW	Mode
4	Enable for restart the PMIC by PWROK drive low when IC is in Self-Work Mode 0: Disable 1: Enable	RW	0
3	Output power down sequence control 0: At the same time; 1: The reverse of the start-up sequence	RW	0
2	Die temperature detect enable 0 : Disable 1: Enable	RW	1
1	The PMIC shut down or not when die temperature is over the warning level 2 (125°C) 0: Not shutdown 1: Shutdown	RW	1
0	Enable for 16s POK shut the PMIC 0: Disable 1: Enable	RW	0

9.2.28. REG 35: Wakeup Pin Function Setting

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3	Wakeup valid signal 0: Low level 1: High level	RW	0
2-0	Wakeup pin function setting bit[2:0] 000: Wakeup IN 001: Wakeup OUT 010: Drive low 011: Drive high(VINT) 1xx: Floating	RW	000

9.2.29. REG 36: POK Setting

Default: 59H

Reset: bit[3] is system reset, the others is Power on reset

Bit	Description	R/W	Default
7-6	ONLEVEL setting 1-0 00: 128ms 01: 1s 10: 2s 11: 3s	RW	01
5-4	IRQLEVEL setting 1-0 00: 1s 01: 1.5s 10: 2s 11: 2.5s	RW	01
3	Enable bit for the function which will shut down the PMIC when POK is larger than OFFLEVEL 0: Disable 1: Enable	RW	1
2	The PMIC auto turn on or not when it shut down after OFFLEVEL POK 0: Not turn on 1: Auto turn on	RW	0
1-0	OFFLEVEL setting 1-0 00: 4s 01: 6s 10: 8s 11: 10s	RW	01

9.2.30. REG 3E: Interface Mode Select

Default: 00H

Reset: power on reset

Bit	Description	R/W	Default
-----	-------------	-----	---------

7-0	Interface mode select 0111,1100(7CH): RSB Others: TWSI	RW	00H
-----	--	----	-----

9.2.31. REG 3F: Special Control Register

Default: 00H

Reset: system on reset

Bit	Description	R/W	Default
7	Power disable control. Write "1" to this bit will power off the PMIC, and this bit will be cleared itself. (The function is same as REG32[7], Which is used to control multiple PMICs to turn off at the same time in generally.)	RW	0
6	After writing 1, the value of the buffer register is exported to REG10/11. And then, the output is automatically cleared and REG1F[6] is set to 0.	RW	0
5	Soft Power Wakeup. Write "1" to this bit, the output power will wake up, and this bit will be cleared itself (The function is same as REG31[5], Which is used to control multiple chips to wakeup at the same time in generally.)	RW	0
4-0	Reserved	RW	00000

9.2.32. REG 40: IRQ Enable1

Default: 03H

Reset: system reset

Bit	Description	R/W	Default
7	Voltage of DCDC-E is under 85% of setting IRQ enable	RW	0
6	Voltage of DCDC-D is under 85% of setting IRQ enable	RW	0
5	Voltage of DCDC-C is under 85% of setting IRQ enable	RW	0
4	Voltage of DCDC-B is under 85% of setting IRQ enable	RW	0
3	Voltage of DCDC-A is under 85% of setting IRQ enable	RW	0
2	Reserved	RW	0
1	Die temperature is over the warning level 2 IRQ enable	RW	1
0	Die temperature is over the warning level 1 IRQ enable	RW	1

9.2.33. REG 41: IRQ Enable2

Default: 03H

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6	POKPIRQ enable	RW	0
5	POKNIRQ enable	RW	0
4	Wakeup source enable in wakeup pin when it's wakeup IN	RW	1
3-2	Reserved	RW	00
1	POKSIRQ enable	RW	1
0	POKLIRQ enable	RW	1

9.2.34. REG 48: IRQ Status1

Default: 00H

Reset: system reset (reset signal is controlled by REGF2[7])

Bit	Description	R/W	Default
7	Voltage of DCDC-E is under 85% of setting, writing 1 to this bit or the output rise to normal will clear it	RW	0
6	Voltage of DCDC-D is under 85% of setting, writing 1 to this bit or the output rise to normal will clear it	RW	0
5	Voltage of DCDC-C is under 85% of setting, writing 1 to this bit or the output rise to normal will clear it	RW	0
4	Voltage of DCDC-B is under 85% of setting, writing 1 to this bit or the output rise to normal will clear it	RW	0
3	Voltage of DCDC-A is under 85% of setting, writing 1 to this bit or the output rise to normal will clear it	RW	0
2	Reserved	RW	00
1	Die temperature is over the warning level 2 Writing 1 to it or temperature drop to level 2 will clear it	RW	0
0	Die temperature is over the warning level 1 Writing 1 to it or temperature drop to level 1 will clear it	RW	0

9.2.35. REG 49: IRQ Status2

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6	POKPIRQ Writing 1 to it will clear it	RW	0
5	POKNIRQ Writing 1 to it will clear it	RW	0
4	Wakeup source is detected by wakeup pin Writing 1 to it will clear it	RW	0
3-2	Reserved	RW	00
1	POKSIRQ Writing 1 to it will clear it	RW	0
0	POKLIRQ Writing 1 to it will clear it	RW	0

9.2.36. REG F3: VREF & Temperature Warning Level Setting

Default: 01H

Reset: Bit4 system reset, other power on reset

Bit	Description	R/W	Default
7	Control VREF power-saving or not when the PMIC is on 0: Not saving 1: Auto saving	RW	0

6-5	VREF power-saving cycle set 00: 16ms 01: 32ms 10: 48ms 11:64ms	RW	00
4	VREF output resister control for voltage sense 0: 20K 1: <1K	RW	0
3-2	Reserved	RW	00
1-0	Temperature warning level 1 & level 2 setting 01: Corresponding level 1 = 125°C, level 2 = 135°C steps: 10°C, level1&2 linkage(fixed error: 10)	RW	01

9.2.37. REG FE: Serial Interface Address Extension

Default: UDF

Bit	Description	R/W
7	Extended address: bit3:0 (which can't be set to full 1) Bit3:2 = 00 Bit[1] is customizable, Default value is 0. MODESET=VINT/Floating(master/self-work mode): bit0=0 MODESET=GND(slave mode): bit0=1	R
6		R
5		R
4		R
3-0	Not design	

9.2.38. REG FF: Register Address Extension

Default: UDF

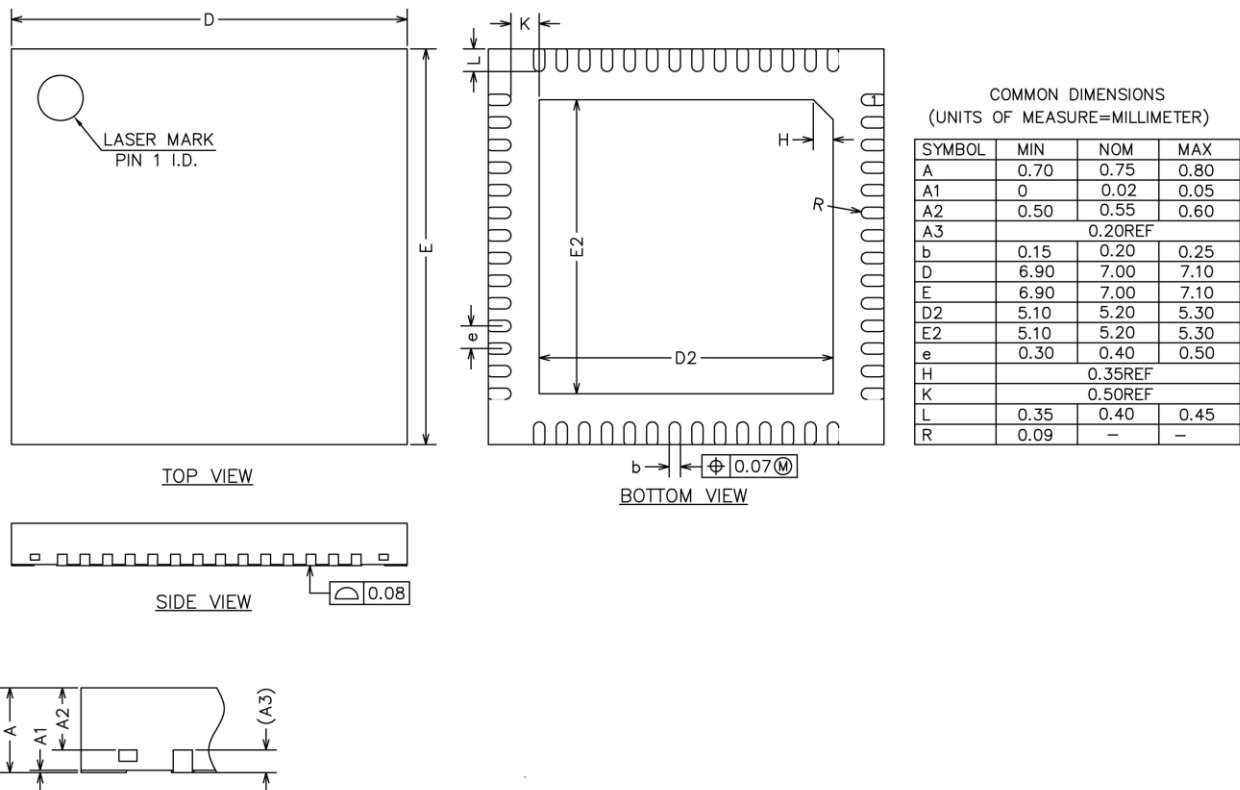
Reset: system reset

Bit	Description	R/W	Default
7-4	The dynamic value of extended address. Read and Write the chip when it is the same as 0xFE[7:4].	RW	0000
3-0	Register address extension bit, map to the bit[11:8] of the address	RW	0000

NOTE: No matter what the high value is, and as long as the address of lower 8-bit is 0xFF, and the register will respond.

10. Package

AXP805 package is QFN7*7, 56-pin.



Order Information:

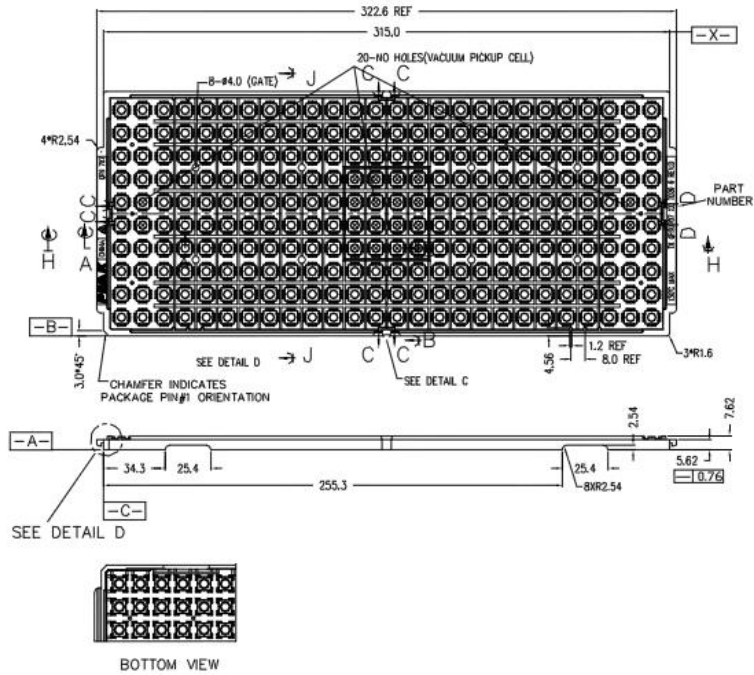
Type	Quantity	Part Number
Tray	260Ppcs/Tray 10Trays/package	AXP805

Marking information:

The first five stand for LOT, as long as the first five number is same, then the lot is same. The six and seven stand for IC version, the last four is related to package information.

Tray Information:

Item	Color	Size
Aluminum foil bags	Silvery White	540*300*0.14mm
Pearl cotton cushion(Vacuum bag)	White	12*680*185mm
Pearl cotton cushion(The Gap between vacuum bag and inside box)	White	Left-Right: 12*180*85mm Front-Back: 12*305*70mm
Inside Box	White	396*196*96mm
Outside Box	White	419*413*319mm



NOTES :

1. MATERIAL - PP6
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TOLERANCES - X.X=±0.25
- X.XX=±0.13
DRAFT ANGLE FOR REFERENCE UNLESS OTHERWISE SPECIFIED.
4. ESD - SURFACE RESISTIVITY - 10^5 TO 10^{11} OHMS/SQ.
5. FOR PACKAGE - QFN 7X7
6. PART NO. : TX QFN0707 1.0 1026 6 REV.D (PLEASE INDICATE ON PURCHASE ORDER).
7. DATECODE AT TRAY BOTTOM SIDE.

Mounting Conditions:

